What is claimed is:

1. A display control device comprising:

a display memory which is capable of storing display data for a display device and into which display data are written in a prescribed number of bits at a time, the display control device successively reading the display data out of the display memory and forming and supplying a drive signal to the display device,

wherein said display memory includes:

a memory array provided with a plurality of memory cells arranged in a matrix form,

a plurality of word lines to which selection terminals for the memory cells are connected,

a plurality of bit lines which are arranged in a direction to cross the word lines and to which data input/output nodes for the memory cells are connected, and

input transfer means and output transfer means being connected to said bit lines, data transferring by said input transfer means resulting in writing of data into the memory cells connected to a word line in a selected state, and data transferring by said output transfer means resulting in reading of data out of the memory cells connected to the word line in a selected state, and

wherein said display memory further includes a plurality of first data latch means capable of successively taking in

the display data in said prescribed number of bits at a time, and display data held by the first data latch means can be collectively transferred by said input transfer means to the bit lines of said display memory in a number of bits at a time equal to an integral multiple of (n times) the number of bits of the display data taken into the first data latch means.

2. The display control device according to Claim 1, further comprising:

a plurality of second data latch means capable of taking in display data held by said first data latch means in a number of bits at a time equal to an integral multiple of the number of bits of the display data taken into said first data latch means,

wherein said input transfer means are configured to be capable of transferring display data held by the second data latch means to the bit lines of said display memory in a number of bits at a time equal to an integral multiple of (n times) the number of bits of the display data taken into said first data latch means.

3. The display control device according to Claim 2, wherein transferring of data by said input transfer means to the bit lines of said display memory takes place at the same timing as the final data taken into said first data latch means.

4. The display control device according to Claim 3, wherein the number of said first data latch means is an integral

multiple further of said n times.

5. The display control device according to Claim 4, further comprising a mask setting means capable of setting the number of bits of data to be transferred by said input transfer means to the bit lines of said display memory, wherein said input transfer means is controlled on the basis of the set information of the mask setting means.

6. The display control device according to Claim 5, wherein said mask setting means can set the start address of write data in a range of consecutive addresses and the quantity of data to be masked from that start address and the end address of the same and the quantity of data to be masked from that end address.

7. The display control device according to Claim 6, further comprising:

segment drive means for generating signals for driving segment electrodes of an external liquid crystal display device on the basis of display data read out of said display memory,

wherein said display control device is configured as a semiconductor integrated circuit over a single semiconductor chip.

8. A mobile electronic apparatus comprising:

the display control device according to Claim 1;

a data processing unit for generating display data to be written into said display memory and setting information

on their writing position; and

a display device for carrying out displaying with a display drive signal read out of said display memory and formed by said display control device on the basis of the display data.

9. The mobile electronic apparatus according to Claim 8, wherein said display device is a dot matrix type liquid crystal display device.

10. The mobile electronic apparatus according to Claim 15,

wherein said display control device comprises a segment drive means for generating signals for driving segment electrodes of said liquid crystal display device, and a common electrode drive circuit for generating a signal for driving common electrodes of said liquid crystal display device is configured as a semiconductor integrated circuit over a separate semiconductor chip from the semiconductor chip over which said display control device is formed, and the common electrode drive circuit is configured of an element higher in withstand voltage than the elements constituting said display control device.

11. A display control device formed over a single semiconductor substrate, comprising:

a memory for storing display data to be displayed on a liquid crystal panel;

a k-bit first external terminal to which display data

to be stored in said memory are supplied from a microprocessor;

a plurality of second external terminals for outputting drive signals for driving said liquid crystal panel on the basis of m-bit read data from said memory;

a first latch circuit connected between the input of said memory and said first external terminal and capable of storing m-bit display data; and

a transfer circuit for selecting, for each integral multiple (multiple by n) of said k bits, display data of not more than said m bits (k · n) in said first latch circuit and transferring them to bit lines of said memory.

12. The display control device according to Claim 11, further comprising:

a second latch circuit provided between said transfer circuit and said first latch circuit and capable of storing said m-bit display data,

said second latch circuit outputting display data of said number of bits (k · n) to said transfer circuit.

13. The display control device according to Claim 11,

wherein said display control device has a control register for setting a first operating mode and a second operating mode,

wherein the mode of writing into said memory is set in said first operating mode in response to the setting of a first value into said control register,

wherein the mode of writing into said memory is set in said second operating mode in response to the setting of a second value into said control register, and

wherein said transfer circuit transfers, for each integral multiple (multiple by n) of said k bits stored in said first latch circuit, said display data to bit lines of said memory in response to setting into said first operating mode and, for every k bits stored in said first latch circuit, said display data to bit lines of said memory in response to setting into said second operating mode.

14. The display control device according to Claim 13, further comprising a segment driver for forming a drive signal to be supplied to a segment line of said liquid crystal panel in response to read data from said memory.

15. The display control device according to Claim 14, further comprising a gradation voltage generator and a gradation voltage select circuit for selecting, in response to read data from said memory, a desired gradation voltage out of a plurality of gradation voltages generated by said gradation voltage generator.

16. The display control device according to Claim 15, further comprising a common driver for forming a drive signal for periodically driving a plurality of common lines of said liquid crystal panel.

17. The display control device according to Claim 15,

further comprising a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory,

said transfer circuit being controlled on the basis of information set in said mask setting circuit.

18. A display control device, formed over a single semiconductor substrate, comprising:

a memory for storing display data to be displayed on a liquid crystal panel capable of color displaying;

a k-bit first external terminal to which display data to be stored in said memory are supplied from a microprocessor;

a plurality of second external terminals for outputting drive signals for driving said liquid crystal panel on the basis of m-bit read data from said memory;

a first latch circuit connected between the input of said memory and said first external terminal and capable of storing m-bit display data;

a transfer circuit for selecting, for each integral multiple (multiple by n) of said k bits, display data of not more than said m bits ($k \cdot n$) in said first latch circuit and transferring them to bit lines of said memory;

a gradation voltage generator;

a gradation voltage select circuit for selecting, in response to read data from said memory, a desired gradation voltage out of a plurality of gradation voltages generated by

said gradation voltage generator; and

a segment driver for forming a drive signal to be supplied to a segment line of said liquid crystal panel on the basis of said selected gradation voltage.

19. The display control device according to Claim 18, further comprising a common driver for forming a drive signal for periodically driving a plurality of common lines of said liquid crystal panel.

20. The display control device according to Claim 18, further comprising a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory,

said transfer circuit being controlled on the basis of information set in said mask setting circuit.

21. A mobile electronic apparatus comprising:

a liquid crystal panel including a plurality of common electrodes, a plurality of segment electrodes, and a plurality of dots driving by the difference in potential between said plurality of common electrodes and said plurality of segment electrodes;

a data processing unit for generating display data to be displayed on said liquid crystal panel; and

a display control device,

wherein said display control device includes:

a memory for storing display data to be displayed

on said liquid crystal panel;

a k-bit first external terminal to which display data to be stored in said memory are supplied from said data processing unit;

a plurality of second external terminals for outputting drive signals for driving said liquid crystal panel on the basis of m-bit read data from said memory;

a first latch circuit connected between the input of said memory and said first external terminal and capable of storing m-bit display data;

a transfer circuit for selecting, for each integral multiple (multiple by n) of said k bits, display data of not more than said m bits ($k \cdot n$) in said first latch circuit and transferring them to bit lines of said memory;

a gradation voltage generator;

a gradation voltage select circuit for selecting, in response to read data from said memory, a desired gradation voltage out of a plurality of gradation voltages generated by said gradation voltage generator; and

a segment driver for forming a drive signal to be supplied to a segment line of said liquid crystal panel on the basis of said selected gradation voltage.

22. The mobile electronic apparatus according to Claim 21, wherein said display control device further comprises a common driver for forming a drive signal for periodically

driving a plurality of common lines of said liquid crystal panel.

23. The mobile electronic apparatus according to Claim 21, wherein said display control device further comprises a mask setting circuit capable of setting the number of bits of data to be supplied to bit lines of said memory,

said transfer circuit being controlled on the basis of information set in said mask setting circuit.

24. The mobile electronic apparatus according to Claim 21, wherein said liquid crystal panel is capable of color displaying in which each picture element comprises three dots of red, green and blue.